WHAT IS CLAIMED IS:

1. A silicon controlled rectifier comprising:

a substrate;

an epitaxial layer of a first conductivity type formed on the substrate, the epitaxial layer having a top surface and a dopant concentration;

a first semiconductor region of the second conductivity type formed in the epitaxial layer, the first semiconductor region contacting the top surface of the epitaxial layer; and

a second semiconductor region of the first conductivity type formed in the epitaxial layer, the second semiconductor region contacting the top surface of the epitaxial layer, being spaced apart from the first semiconductor region, and having a dopant concentration greater than the dopant concentration of the epitaxial layer.

2. The rectifier of claim 1 and further comprising:

a first polysilicon region that contacts the top surface of the epitaxial layer over the first semiconductor region, the first polysilicon region having the second conductivity type; and

a second polysilicon region that contacts the top surface of the epitaxial layer over the second semiconductor region, the second polysilicon region being spaced apart from the first polysilicon region and having a region of the second conductivity type.

3. The rectifier of claim 2 and further comprising a third semiconductor region formed in the second semiconductor region, the third semiconductor region having the second conductivity type.

4. The rectifier of claim 3 and further comprising a third polysilicon region that contacts the top surface of the epitaxial layer over the first semiconductor region, the third polysilicon region having the first conductivity type and being spaced apart from the first and second polysilicon regions.

5. The rectifier of claim 4 wherein the first and third polysilicon regions are electrically connected together.

6. The rectifier of claim 3 wherein the second semiconductor region has a high dopant concentration region and a low dopant concentration region that contacts the high dopant concentration region.

7. The rectifier of claim 6 wherein the second polysilicon region contacts the low dopant concentration region.

8. The rectifier of claim 6 and further comprising a pn junction that lies between the low dopant concentration region and the second polysilicon region.

9. The rectifier of claim 6 wherein the second polysilicon region is spaced apart from the epitaxial layer.

10. The rectifier of claim 6 wherein the third layer of polysilicon has a dopant concentration that is greater than a dopant concentration of the high dopant concentration region.

11. The rectifier of claim 6 wherein the third layer of polysilicon has a dopant concentration that is substantially equal to a dopant concentration of the high dopant concentration region.

12. The rectifier of claim 3 and further comprising a buried region of the first conductivity type, the buried region contacting the epitaxial layer.

13. The rectifier of claim 6 and further comprising:

a layer of isolation material formed over the epitaxial layer;

a first contact formed through the layer of isolation material to make an electrical connection with the first polysilicon region;

a second contact formed through the layer of isolation material to make an electrical connection with the second polysilicon region; and

a third contact formed through the layer of isolation material to make an electrical connection with the third polysilicon region.

14. A method of forming a silicon controlled rectifier, the rectifier having a substrate, an epitaxial layer of a first conductivity type formed on the substrate, a first semiconductor region of the second conductivity type formed in the epitaxial layer, and a second semiconductor region of the first conductivity type in the epitaxial layer, the epitaxial layer having a top surface, the first and second semiconductor regions contacting the top surface of the epitaxial layer, the method comprising the steps of:

forming a layer of polysilicon that contacts the top surface of the epitaxial layer; and

doping and etching the layer of polysilicon to form a first polysilicon region over the first semiconductor region, a second

polysilicon region over the first semiconductor region, and a third polysilicon region over the second semiconductor region.

15. The method of claim 14 wherein the first semiconductor region has the first conductivity type, the second semiconductor region has the second conductivity type, and the third semiconductor region has the second conductivity type.

16. The method of claim 15 wherein the third semiconductor region also has the first conductivity type.

17. The method of claim 16 and further comprising the steps of:

forming a layer of isolation material over the first, second, and third polysilicon regions and the epitaxial layer;

forming a first contact through the layer of isolation material to make an electrical connection with the first polysilicon region;

forming a second contact through the layer of isolation material to make an electrical connection with the second polysilicon region;

forming a third contact through the layer of isolation material to make an electrical connection with the third polysilicon region; and

forming a metal-1 trace on the layer of isolation material that makes an electrical connection with the first and second contacts.

18. The method of claim 17 wherein the silicon controlled rectifier has a buried layer formed in the substrate, the buried layer contacting the epitaxial layer and having a same conductivity type.